Docket No.: 067471-0011 **PATENT**

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of	:	Customer Number: 53080
Masato SUZUKI et al.	:	Confirmation Number: 9431
Application No.: 09/662,484	:	Group Art Unit: 2454
Filed: September 14, 2000	:	Examiner: COULTER, KENNETH R.

For: VARIABLE ADDRESS LENGTH COMPILER AND PROCESSOR IMPROVED IN ADDRESS MANAGEMENT

SUPPLEMENTAL DECLARATION IN REISSUE APPLICATION PURSUANT TO 37 C.F.R. § 1.175(b)

1. We, Masato Suzuki, Hiroshi Kamiyama, and Shinya Miyaji, all citizens of Japan, hereby declare that we are the original, first and joint inventors of the subject matter of U.S. Patent No. 5,809,306 (the '306 patent) entitled VARIABLE ADDRESS LENGTH COMPILER AND PR0CESSOR IMPROVED IN ADDRESS MANAGEMENT, which issued September 15, 1998, from U.S. application Serial No. 08/587,338, filed January 16, 1996; that we were employed by Matsushita Electric Industrial Co., Ltd. of Osaka, Japan (now named Panasonic Corporation as the result of a corporate name change) at the time this Reissue application was filed; that Panasonic Corporation is the Assignee of the entire interest of this Reissue application; that at the time this Reissue application was filed we were engaged in the design of electronic technology and data processors as described in the '306 patent; that we do not know and do not believe that the invention was ever known or used in the United States before our invention; and that we are the declarants, applicants and patentees, referred to hereinafter.

2. That we believe we are the original/first inventors of the subject matter of the invention, which is claimed and for which a reissue patent is sought in this Reissue application.

3. That we believe the '306 patent to be wholly or partly inoperative or invalid, by reason of our claiming less than we had a right to claim. Specifically, claims 1-61 fail to embody one of the inventive features of the present invention without undue limitations, e.g., a device/method which can perform zero-extending and/or sign-extending of data dependent on whether an instruction designates a given register. We believe this inventive concept is not disclosed or suggested by prior art so as to be patentable without further limitation; whereas claims in the '306 patent include additional limitations, so that we claimed less than we had a right to claim. For example, claim 35 of the '306 patent unnecessarily includes the following limitation:

> ...instruction control means for decoding an instruction to zero-extend M-bit immediate data when said M-bit immediate data are to be stored in said first register means by the decoded instruction and to sign-extend said M-bit immediate data when said M-bit immediate data are to be stored in said second register means by the decoded instruction, said zero-extended and sign-extended N-bit immediate data being outputted in one of two methods, one method being to send the extended N-bit immediate data from their respective extending means to their respective register means directly, the other being to send the same via the operating means to their respective register means, with said instruction including an indication for storing in the first register means and said instruction including an indication for storing in the second register means being of two different kinds of instructions, both kinds of instructions having a same operation code but having different destination operands.

As another example, claim 38 of the '306 patent unnecessarily includes the following limitation:

> ...control means for outputting said M-bit immediate data to said zero-extending means when the first type instruction is detected, and for outputting said M-bit immediate data to said sign-extending means when the second type instruction is detected, said zero-extended N-bit immediate data and sign-extended N-bit immediate data being outputted in one of two methods, one method being to send the extended N-bit immediate data from their respective extending means to their respective register means directly, the other being to send the same via the operating means to their respective register means, with said first-type instruction and said second-type instruction both having a same operation code but having different destination operands.

As yet another example, claim 42 of the '306 patent unnecessarily includes the following limitation:

> [a] data processing method for executing an instruction that includes an operation code to store M-bit immediate data in an N-bit first register and an N-bit second register, both M and N being integers, with M being less than N, said method comprising the steps of: ...
>
> zero-extending said M-bit immediate data to N bits when said decoded instruction designates the first register, and sign-extending said M-bit immediate data to N bits when said decoded instruction designates the second register; and
>
> storing extended N-bit immediate data to the designated register.

4. That we believe that the error regarding our narrow claiming of the invention arose inadvertently and without deceptive intent.

5. That every error in the '306 patent which is corrected by this Reissue application, and is not covered by a prior oath/declaration submitted in this Reissue application, arose without any deceptive intent.

6. In accordance with 35 U.S.C. § 120, we claim the benefit of the filing date of prior US application Serial No. 08/249,157 ('157 application), filed on May 26, 1994, now abandoned (the '306 patent is a continuation of the '157 application); and in accordance with 35 U.S.C. § 119, we claim the benefit of the foreign filing date of Japanese Patent Application No. 5-126212, filed on May 27, 1993, Japanese Patent Application No. 5-129529, filed on May 31, 1993, and Japanese Patent Application No. 5-247154, filed on October 1, 1993. A certified copy of the Japanese priority documents were filed in the '157 application now abandoned.

7. That we have reviewed and understand the contents of this Reissue application, including new claims 80-82, 85, 87-90, and 95 added by amendment, and all subsequent amendments made to these claims.

8. That we acknowledge the duty to disclose information of which we are aware and which is material to the patentability of this Reissue application in accordance with 37 C.F.R. § 1.56(a).

We declare further that all statements made herein of our own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issuing thereon.

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